IN THE SPECIFICATION

Following is a marked-up version of each amended paragraph of the subject patent application. The Examiner is requested to delete the indicated paragraph and replace it with the amended paragraph. The location for each of the deleted and replaced paragraphs is also indicated..

Replace the paragraph beginning on page 4, line 10 and ending on page 5, line 5 with the following.

In an associated method of manufacture, an integrated circuit structure is fabricated by providing a semiconductor layer suitable for device formation and having a surface formed along a first plane. For a first field-effect transistor a first device region is formed in the semiconductor layer, wherein the device region is selected from among a source and a drain region. For a second field-effect transistor a second device region is formed in the semiconductor layer, wherein the second device region is selected from among a source and a drain region and is further isolated from the first device region. Channel regions for each of the first and the second field-effect transistors are formed above the first and the second device regions, respectively, within trenches formed in a plurality of regions over the first and the second device regions. At least two of the plurality of layers comprise doped insulating layers from which source/drain extension regions are formed. A first doped insulating layer of a first conductivity type is formed over the first device region followed by the formation of a doped insulating layer over the entire structure and of the second conductivity type. The second doped insulating layer is then removed in the area overlying the first device region such that the resulting structure comprises the first doped insulating layer over the first device region and the second doped insulting layer over the second device region. Similar[[,]] processing steps are used to form third and fourth doped insulating layers over the first and the second doped insulating layers, respectively. Disposed between the first/second and the third/fourth doped insulating regions is a sacrificial layer that is later removed to allow the formation of gate oxide material in exposed portions of the channel regions.

Add the following paragraph after line 21 on page 5.

Figure 41 is a plan view of certain elements illustrated in the cross-sectional view of Figure 34.

Replace the paragraph beginning on page 7, line 3 and ending on page 7, line 11 with the following.

Referring to Figure 3, there is shown a monocrystalline semiconductor layer 106 ~~100~~ having an exposed major surface 107 ~~106~~ formed along a crystal plane over an upper portion of the layer 106 ~~100~~. An epitaxial layer 108 is grown by conventional means over the exposed major surface 106. In one embodiment, the substrate 106 ~~100~~ is heavily doped with a p-type material (referred to as p+ doping) and the epitaxial layer 108 is lightly p-type doped (referred to as p- doping). The thickness of the substrate 106 ~~100~~ and the epitaxial layer 108, the concentration of the dopant therein, and the type of dopant (e.g., n- type or p-type) are all matters of design choice.

Replace the paragraph beginning on page 9, line 10 and ending on page 9, line 15 with the following.

As shown in Figure 13, a silicon dioxide layer 140 is deposited or formed over the entire device including the silicon dioxide layer ~~136~~ 134 shown in Figure 12. The silicon dioxide layer 140 insulates the source regions 114 and 120 from what will eventually be an overlying gate region. Thus the silicon dioxide layer 140 is composed of a material and has a thickness that is consistent with this insulating objective.

Replace the paragraph beginning on page 9, line 16 and ending on page 10, line 3 with the following.

Next (See Figure 14) an n-doped ~~p-doped~~ tetraethylene-ortho-silicate (PTEOS) layer 142 is formed over the silicon dioxide layer 140. The PTEOS layer 142 is formed by the decomposition of a tetraethyl-ortho silicate precursor or TEOS, i.e., $Si(OC_2H_5)_4$. Decomposition of vaporized liquid TEOS to form a silicon oxide film (referred to herein as a TEOS-deposited oxide) typically occurs by chemical vapor deposition at 650° C to 750° C in an oxygen environment. Such TEOS depositions are known to provide good uniformity in step coverage when needed. Generally, the deposited film is understood to be a non-stoichiometric oxide of silicon, although it is often referred to as silicon dioxide. Including ozone (O_3), e.g., up to 10% of the reacting oxygen, facilitates lower temperature depositions. A typical reaction, including ozone, is performed at 400° and 300° Torr with four standard liters per minutes oxygen, the oxygen comprising 6% ozone, 1.5 standard liters per minute helium and 300 standard cubic centimeters per minutes TEOS. It is known that the

TEOS deposition can include a dopant, in this case an acceptor dopant having a concentration in the rage of about 0.01% to 15%, for forming the PTEOS layer 142 as shown.

Replace the paragraph beginning on page 10, line 15 and ending on page 10, line 21 with the following.

Using these silicon nitride layer 144 as an etch stop, a portion of the PTEOS layer 142 is removed as illustrated in Figure 16. As shown, approximately half of the PTEOS layer 142 is removed, the portion remaining overlying the n region 114. As will be shown further below, the n region 114 forms a source/drain region of an n-channel ~~p-channel~~ MOSFET device; the p region 120 forms a source/drain region of a p-channel ~~an n-channel~~ MOSFET device.

Replace the paragraph beginning on page 13, line 5 and ending on page 13, line 20 with the following.

Referring to Figure 24, an opening or window 200 is anisotropically etched through the BTEOS layers ~~144~~ 146 and 164, the silicon nitride layers 150 and 154, the sacrificial layer 152 and the silicon dioxide layer 140. An opening or window 202 is anisotropically etched through the silicon dioxide layer 140, the PTEOS layers 142 and 160, the silicon nitride layers 150 and 154 and the sacrificial layer 152. The diameter of each window 200 and 202 is determined by the performance characteristics and size constraints for the device under fabrication and the limitations of the lithographic process utilized to form the windows 200 and 202. The lengths of the windows 200 and 202 (which are also referred to as trenches), i.e., the length being orthogonal to both the horizontal and vertical dimensions in the Figure 24 cross section, is largely a matter of design choice and the window lengths are not necessarily identical. For a given horizontal dimension, the current capacity of the doped region that will be later formed in the windows 200 and 202 increases with increased window length.

Replace the paragraph beginning on page 13, line 21 and ending on page 13, line 26 with the following.

In one embodiment, to clean the silicon on a ~~at the~~ bottom surface, ~~of~~ the windows 200 and 202 are then subjected to a chemical cleaning process (e.g. RCA or Piranha-clean). As a result of this cleaning step, small portions of the insulating layer 140 forming a boundary with the windows

200 and 202 may be removed. The indentations thereby created are artifacts of the process and therefore not shown in Figure 24.

Replace the paragraph beginning on page 15, line 22 and ending on page 16, line 2 with the following.

Depending upon the process used to form the crystalline semiconductor materials 204 and 206, a chemical/mechanical polishing step may be required to planarize the top surface thereof. The end result is illustrated in Figure 25. To prevent ~~diffusion~~ dopants from the PTEOS layer 160 and the BTEOS layer 164 from diffusing upwardly when the source/drain regions ~~extensions~~ are formed later, a silicon nitride layer 207 is formed over the entire structure, as shown in Figure 25. Windows are then etched in the silicon nitride layer 207 in preparation for the forming the next layer in the structure, i.e., a source/drain layer that must be in electrical contact with the crystalline semiconductor materials 204 and 206.

Replace the paragraph beginning on page 16, line 3 and ending on page 16, line 17 with the following.

A conformal polysilicon layer 208 is formed over the silicon nitride layer 207 and the crystalline semiconductor materials 204 and 206. See Figure 26. The polysilicon layer 208 provides a self-aligned top contact (the drain region in this embodiment). One example of a suitable material for the polysilicon 208 is doped polycrystalline silicon, wherein opposite-type dopants are introduced during separate masking and implanting steps. That is, the left side of the polysilicon layer 208 is masked and ~~acceptor-type~~ donor-type dopants implanted into the right side of the polysilicon layer overlying the n region 114, to create a drain region 208. Then the drain region 208 is masked and ~~donor-type~~ acceptor-type dopants are implanted into the left right side of the polysilicon layer overlying the p region 120, to create a drain region 210. Concentration of the dopant in the drain regions 208 and 210 is greater than about 1×10^{20} atoms/cm^3. Alternatively, the polysilicon layer 210 can be formed in two separate process to form the n-type and the p-type regions.

Replace the paragraph beginning on page 17, line 20 and ending on page 18, line 2 with the following.

The substrate is then subjected to a wet etch (an aqueous hydrofluoric acid) or an isotropic dry etch (e.g., an anhydrous hydrofluoric acid) that removes the exposed remaining portions of the sacrificial layer 152, exposing portions of the crystalline semiconductor materials 204 and 206. The end result is illustrated in Figure 30 where the PTEOS layer 142 and BTEOS layer ~~144~~ 146 remain covered by the etch stop layer 150. On the left side of Figure 30, the BTEOS layer 164 and the drain region 210 are encapsulated by the remaining portions of the etch stop layer 154, 212 and 220. On the right side of Figure 30, the PTEOS layer 160 and the drain region 208 are also encapsulated by the remaining portions of the etch stop layers 154, 212 and 220. Consequently, the remaining portions of the PTEOS layer 160, the BTEOS layer 164, and the drain regions 208 and 210 remain isolated from contact with subsequent etch expedients.

Replace the paragraph beginning on page 18, line 3 and ending on page 18, line 17 with the following.

According to one embodiment of the present invention, a sacrificial layer of thermal silicon dioxide is grown on the exposed surface of the crystalline semiconductor materials 204 and 206, to a thickness of about less than 10 nm. The sacrificial silicon dioxide is then removed using a conventional isotropic etch, e.g., an aqueous hydrofluoric acid. As a result of the formation and then the removal of the sacrificial silicon dioxide, the surface of each of the crystalline semiconductor materials 204 and 206 is smoother and some of the sidewall defects are removed. The etch stop layers 150 and 154 prevent the etch expedient used to removed the thermal silicon dioxide from contacting the BTEOS layers ~~144~~ 146 and 164 and the PTEOS layers 142 and 160. This step is not necessarily required the for the device fabrication but it can be useful for improving the gate dielectric properties by, for example, reducing interface traps. The step may be omitted if the silicon defects are known not to be detrimental for the device being fabricated.

Replace the paragraph beginning on page 18, line 18 and ending on page 19, line 6 with the following.

The exposed portion of the crystalline semiconductor material 204 defines the physical channel length of the p-channel MOSFET device that is being formed. The exposed portion of the crystalline semiconductor material 206 defines the physical channel length of the n-channel device that is being formed. As shown in Figure 31, a layer of gate dielectric 226 is formed on the exposed portion of the crystalline semiconductor material ~~materials~~ 204 and a gate dielectric gate dielectric

227 is formed on the exposed portion of the crystalline semiconductor material 206. Suitable dielectric materials include, for example, thermally-grown silicon dioxide, silicon oxynitride, silicon nitride and metal oxide. The thickness of the gate dielectrics 226 and 227 is ~~are~~ about 1 nm to about 20 nm. One example of a suitable thickness is 6 nm. In one embodiment the silicon dioxide layer forming the gate dielectrics 226 and 227 are grown by heating the integrated structure to a temperature in a range of about 700° C to about 1000° C in an oxygen-containing atmosphere. Other expedients for forming the gate dielectrics 226 and 227 may include chemical vapor deposition, jet vapor deposition or atomic layer deposition, all of which are contemplated as suitable. Conditions for forming the gate dielectrics 226 and 227 of the desired thickness are well known to those skilled in the art.

Replace the paragraph beginning on page 20, line 3 and ending on page 20, line 24 with the following.

Figure 34 shows the finished n- and p-channel MOSFET device structures. P-type dopants are then driven into the crystalline semiconductor material 204 by solid phase diffusion from the BTEOS layers ~~144~~ 146 and 164 to form source/drain extensions 250. N-type dopants are driven into the crystalline semiconductor material 206 by solid phase diffusion from the PTEOS layers 142 and 160 to form source/drain extensions 252 of the p-channel MOSFET device. In the solid phase diffusion process, an oxide (e.g., silicon oxide) serves as the dopant source. At elevated temperatures, the dopant is driven from the doped oxide to the adjacent undoped (or lightly doped) regions of the crystalline semiconductor materials 204 and 206. This technique is advantageous because the doped area, and thus the extensions, are defined by the interface between the crystalline semiconductor materials 204 and 206 and the BTEOS/PTEOS layers 146 ~~144~~ and 164/142 and 160. This process also allows the formation of self-aligned source/drain extensions (i.e., the source/drain extensions are aligned with the gate). Examples of solid phase diffusion techniques are described in Ono, M., et al, Sub-50 nm Gate Length N-MOSFETs with 1 nm Phosphorus Source and Drain Junctions, IEDM 93, pp. 119-122, (1993) and Saito M., et al, An SPDD D-MOSFET Structure Suitable for 0.1 and Sub 0.1 Micron Channel Length and Its Electrical Characteristics, IEDM 92, pp. 897-900 (1992), which are hereby incorporated by reference.

Replace the paragraph beginning on page 20, line 25 and ending on page 21, line 17 with the following.

The concentration of the dopant in the source/drain extensions 250 and 252 is typically about at least 1 x $10^{19}/cm^3$, with dopants concentrations of about 5 x $10^{19}/cm^3$ contemplated as advantageous. Using this solid phase diffusion technique, very shallow source and drain extensions are obtainable. The source/drain extensions 250 and 252 are shown as penetrating into the crystalline semiconductor materials 204 and 206, respectively, preferably less than one-half width of the crystalline semiconductor materials 204 and 206. Limiting the dopant penetrations in this manner avoids significant overlap of the doped regions from opposite sides of the crystalline semiconductor materials 204 and 206. Also, the distance that the source/drain extension 250 and 252 extend under the gate is preferably limited to one-fourth of the gate length. In the resulting structure, the net concentration of dopants in the source/drain extensions 250 and 252 are of the opposite type than present in the channels to 260 and 262. The silicon dioxide ~~oxide~~ layer 140 prohibits the downward movement of the dopants from the BTEOS layer 146 ~~144~~ and the PTEOS layer 142 into the p-type region 120 and the n-type region 114 ~~144~~, respectively, and then upwardly into the crystalline semiconductor materials 204 and 206 respectively. The etch stop layer 150 prevents the upward diffusion of the dopants from the BTEOS layer ~~144~~ 146 into the gate 240 and from the PTEOS layer 142 into the gate 242. The etch stop layer 154 prevents the downward diffusion of dopants from the BTEOS layer 164 into the gate 240 and from the PTEOS layer 160 into the gate 242.

Replace the paragraph beginning on page 21, line 18 and ending on page 21, line 21 with the following.

To form the CMOS circuit of Figure 2, the drain regions 208 and 210 are electrically connected in the third dimension, i.e., outside of the two dimensions depicted in the cross- sectional views of the Figures. Figure 41 illustrates a PMOSFET 288 (comprising the elements on the left side of Figure 34) and an NMOSFET 289 (comprising the elements on the right side of Figure 34) in a plan view. The drain regions 208 and 210 are connected by vertical conductive vias 291 and 292 and a conductor 293 formed in a metallization layer overlying the PMOSFET 288 and the NMOSFET 289. The electrical connection between the drain regions 208 and 210 is similar to the connection between the drain of PMOS 2 and the drain of NMOS 4 of Figure 2. The source contacts are also accessed in the third dimension.

Replace the two-paragraph Abstract on page 30 with the following single paragraph Abstract.

ABSTRACT

An architecture and process for forming CMOS vertical replacement gate metal oxide semiconductor field-effect transistors is disclosed. The integrated circuit structure includes a semiconductor area with a major surface formed along a plane and first and second source/drain dopes regions formed in the surface. An insulating trench is formed between the first and second source/drain regions. A third doped region forming a channel of a different conductivity type than the first source/drain region is positioned over the first source/drain region. A fourth doped region is formed over the second source/drain region, having an opposite conductivity type with respect to the second source/drain region, and forming a channel region. Fifth and sixth source/drain regions are formed respectively over the third and fourth doped regions. ——In an associated method of manufacturing the semiconductor device, first and second source/drain regions are formed in the semiconductor layer, followed by the formation of third and fourth doped regions forming the channel. Fifth and sixth doped regions are then formed over the channels to complete the structure. An insulating region is formed between the first and the second source/drain regions to isolate these regions of opposite conductivity type.